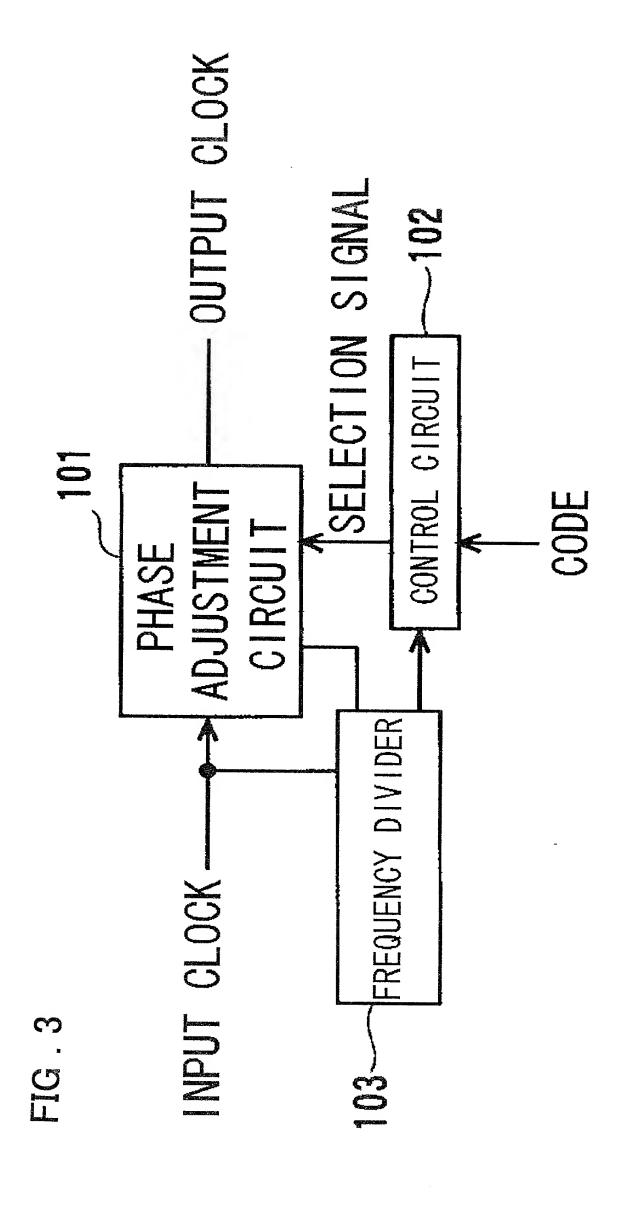
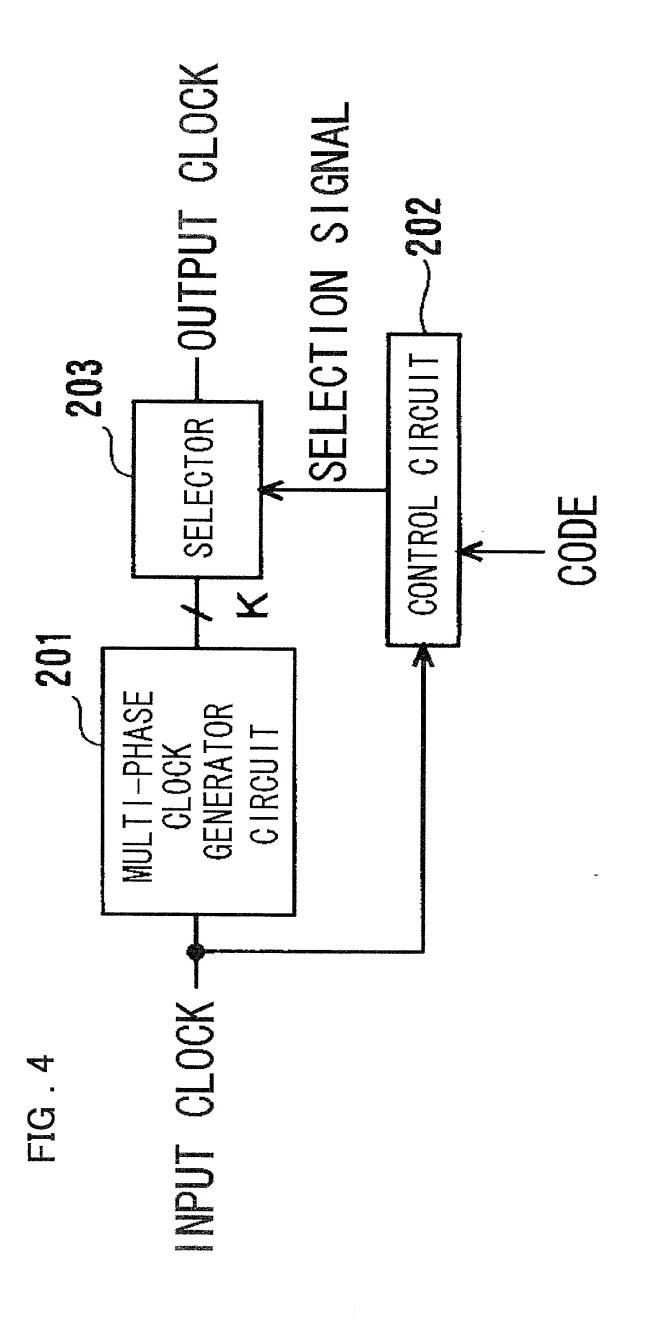
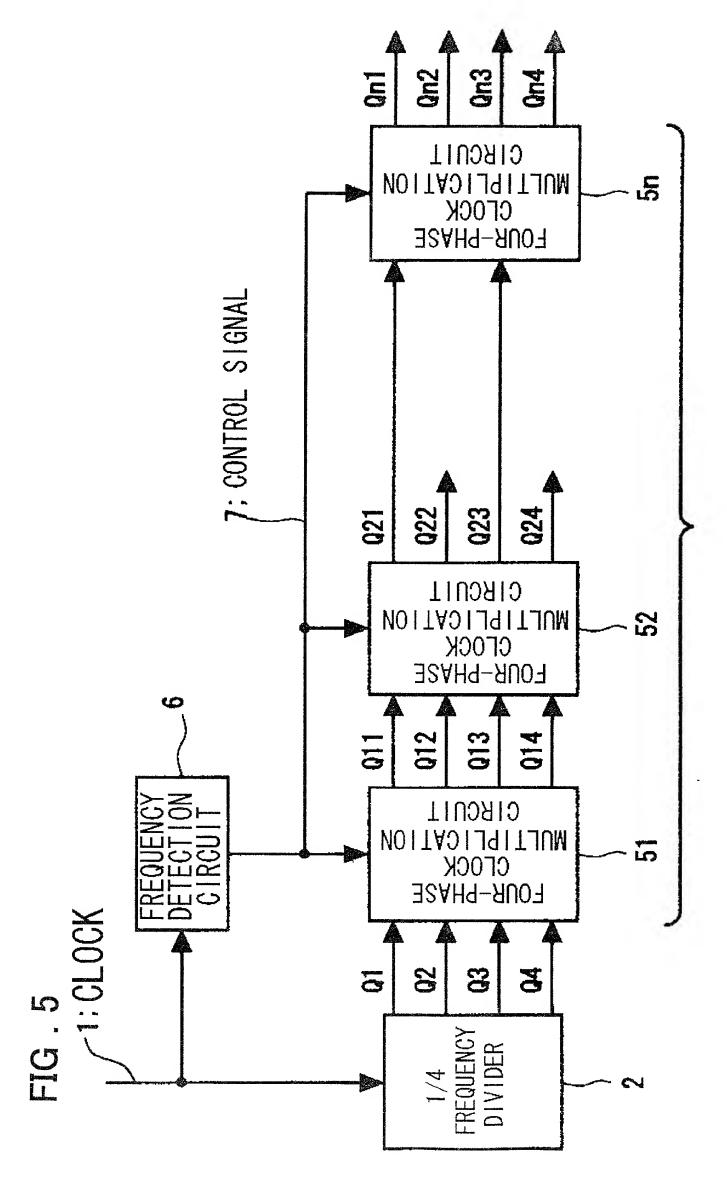


PER 10D RAT 10 = (tCK+10)/tCK







5; FOUR-PHASE CLOCK MULTIPLICATION CIRCUIT

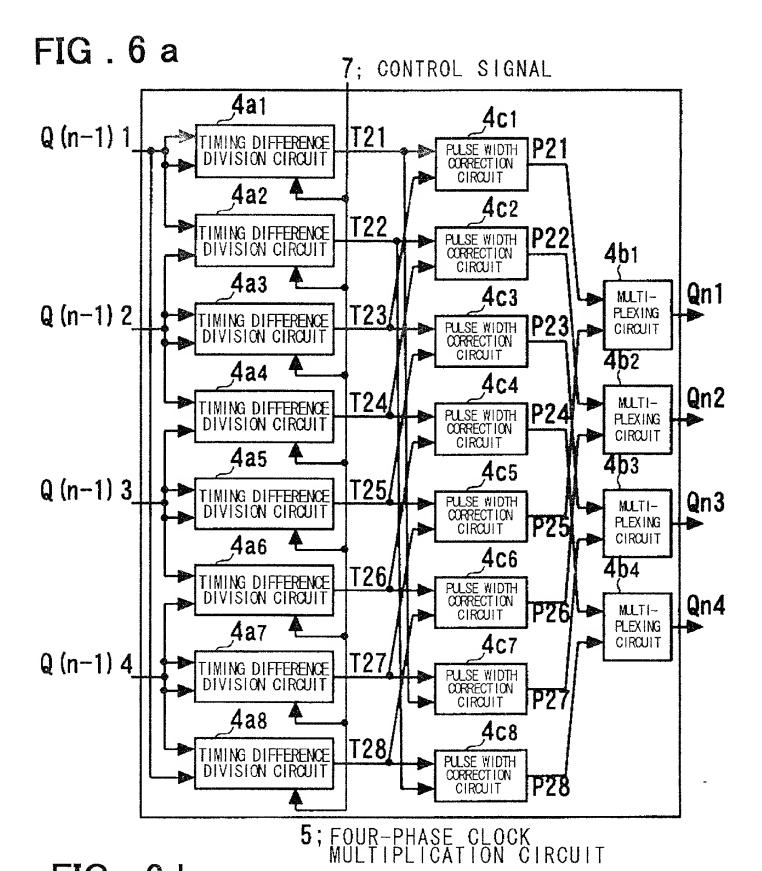
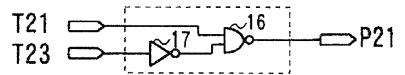


FIG.6b



PULSE WIDTH CORRECTION CIRCUIT

FIG.6c

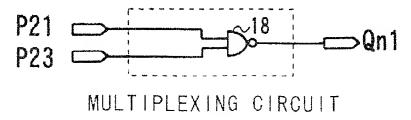


FIG. 7

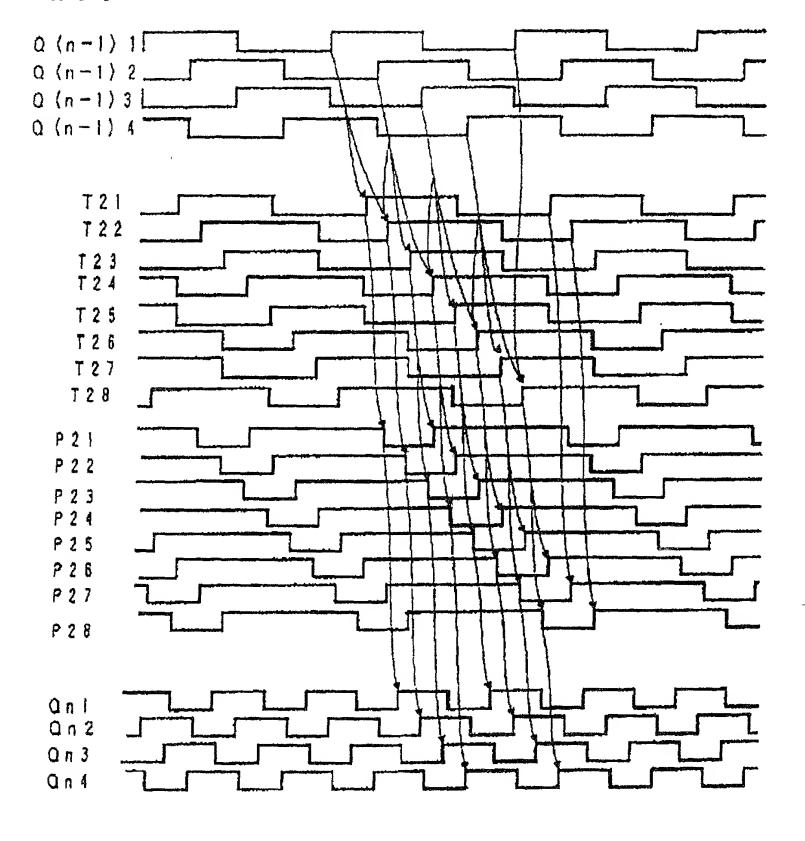


FIG . 8 a

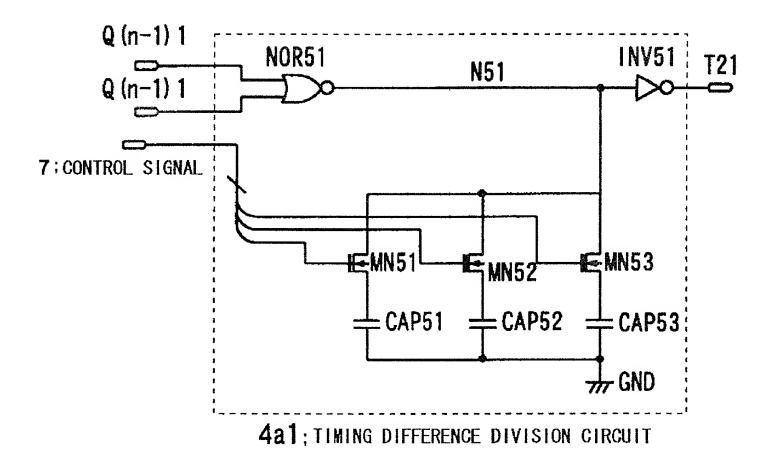


FIG . 8 b

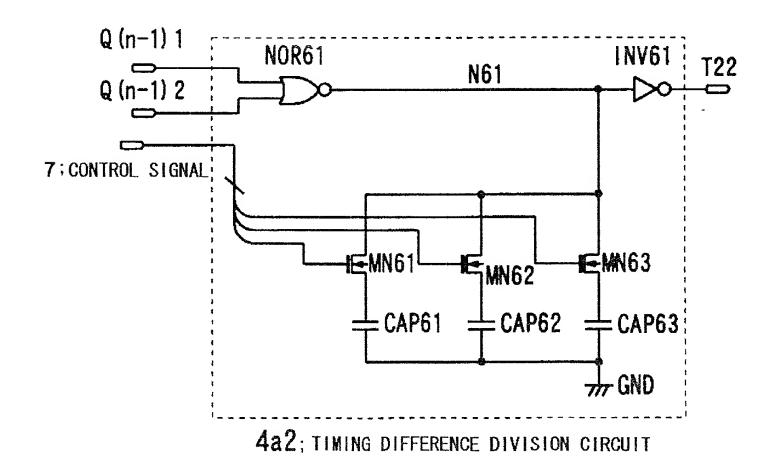


FIG.9

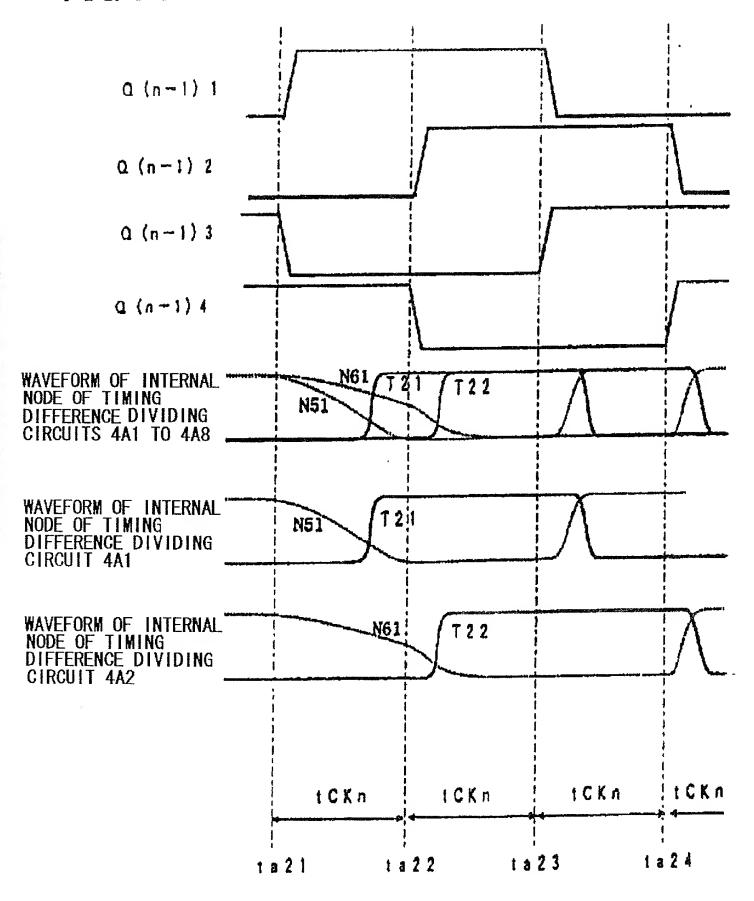


FIG . 10

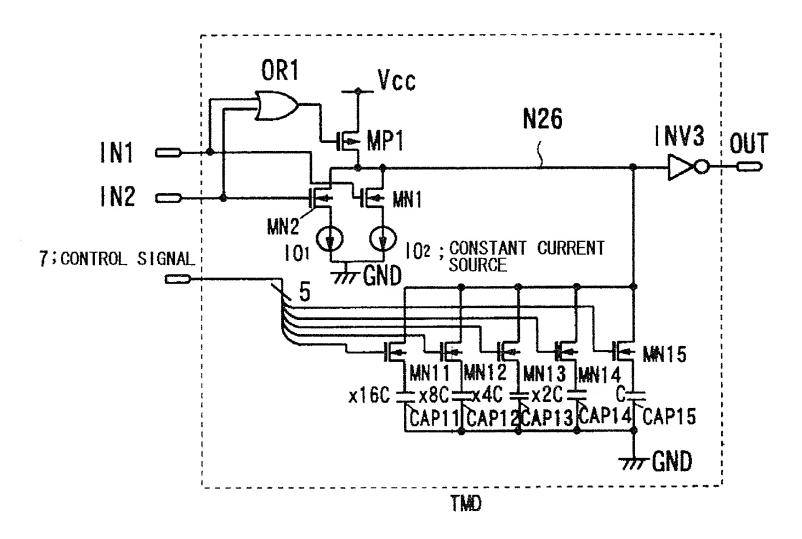


FIG . 11 a

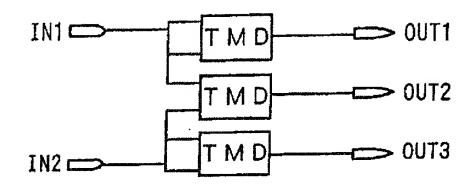


FIG . 11 b

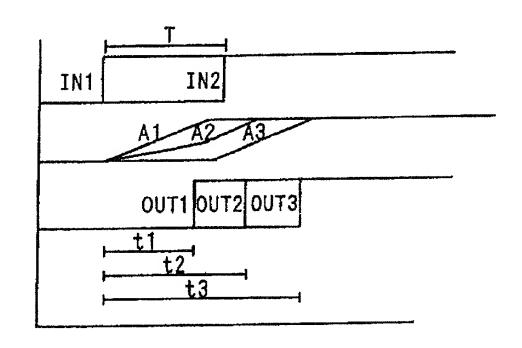
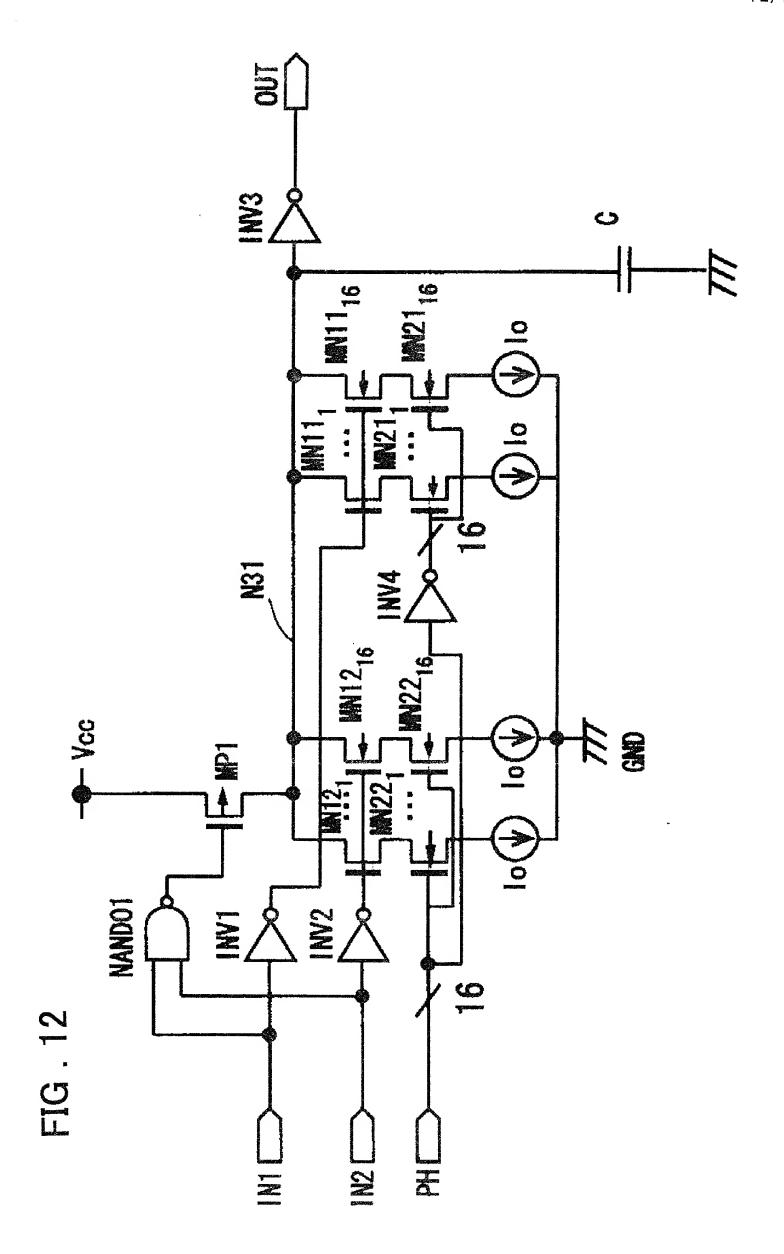


FIG . 11 c

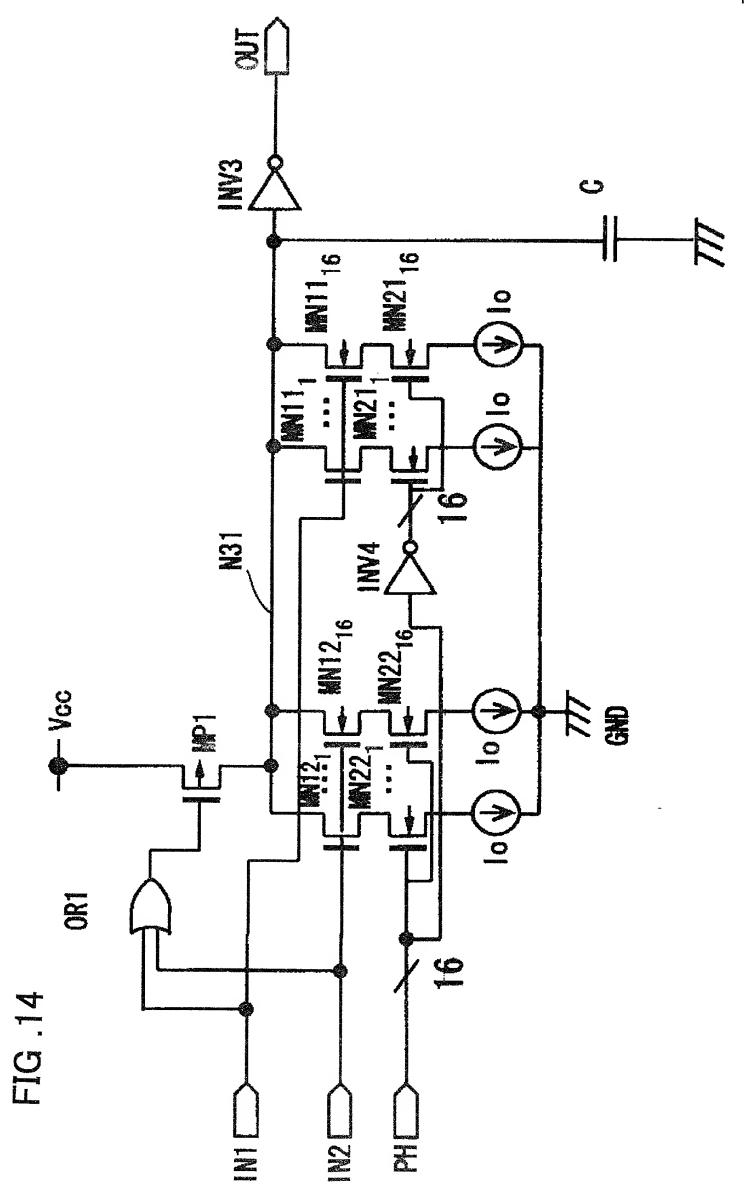


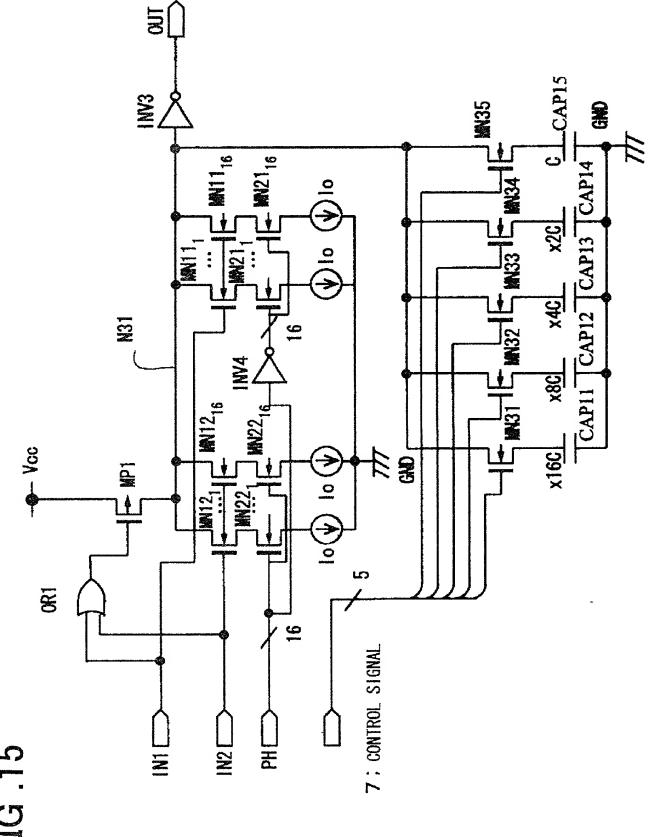
CAP11 CAP12 CAP13

- Vcc NANDO1 IN V 16 7; CONTROL SIGNAL FIG. 13 문

\$(

M31





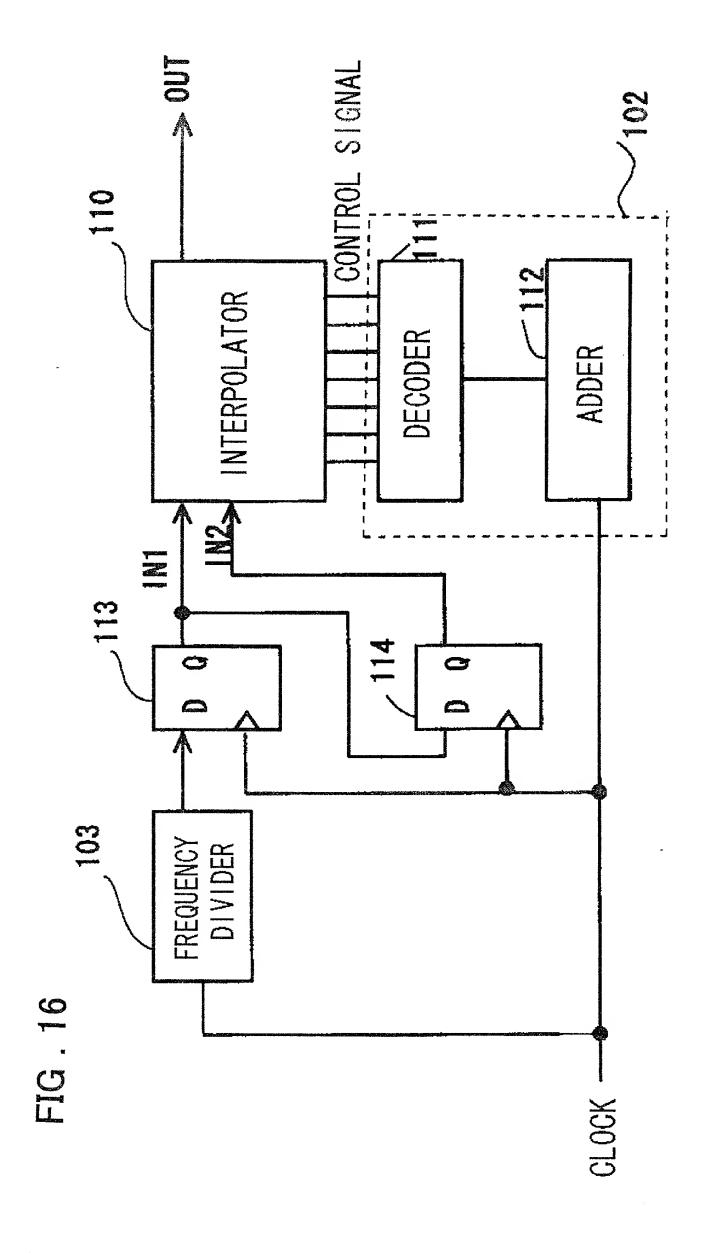


FIG. 17

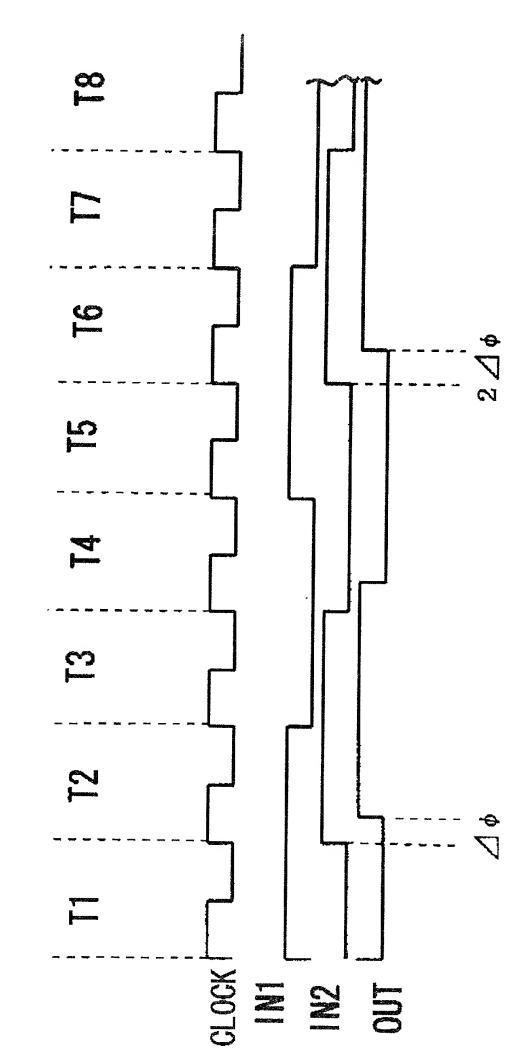
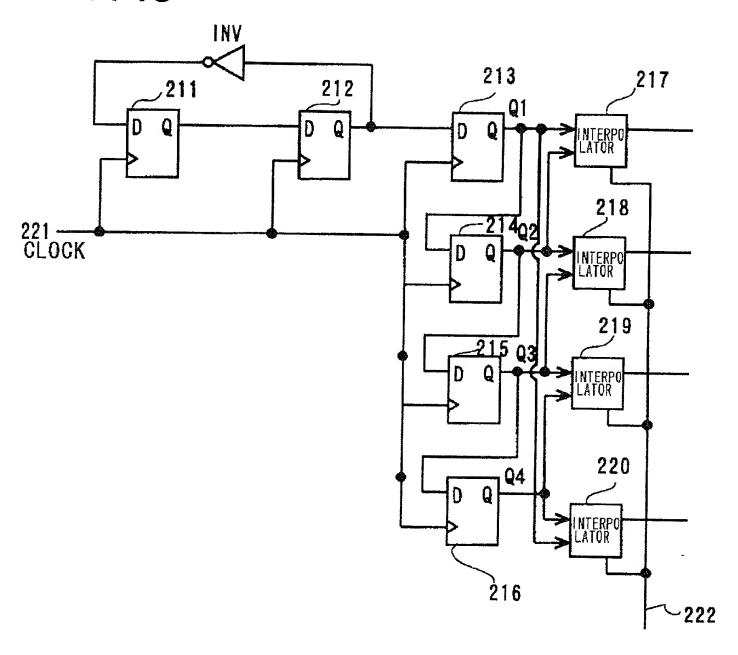
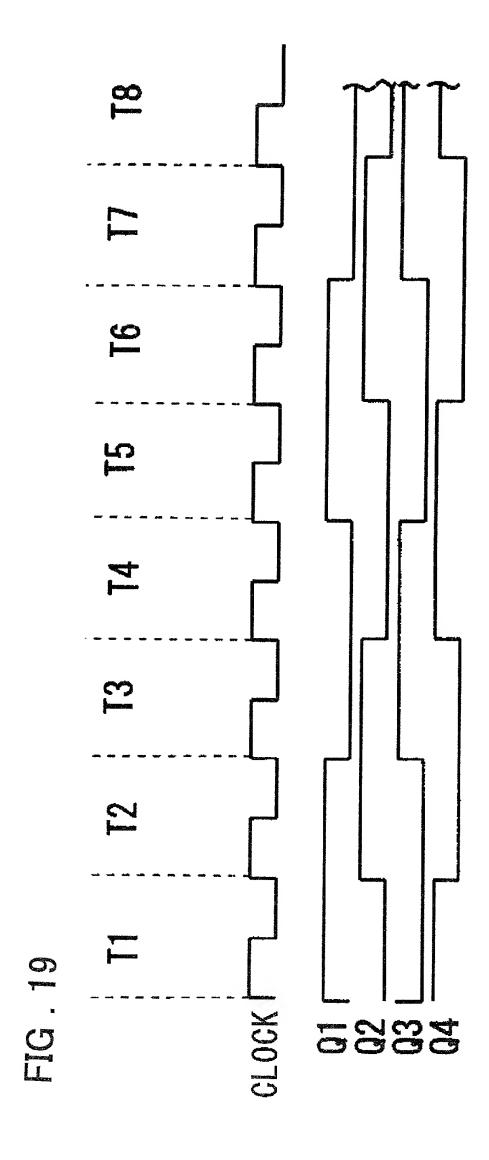
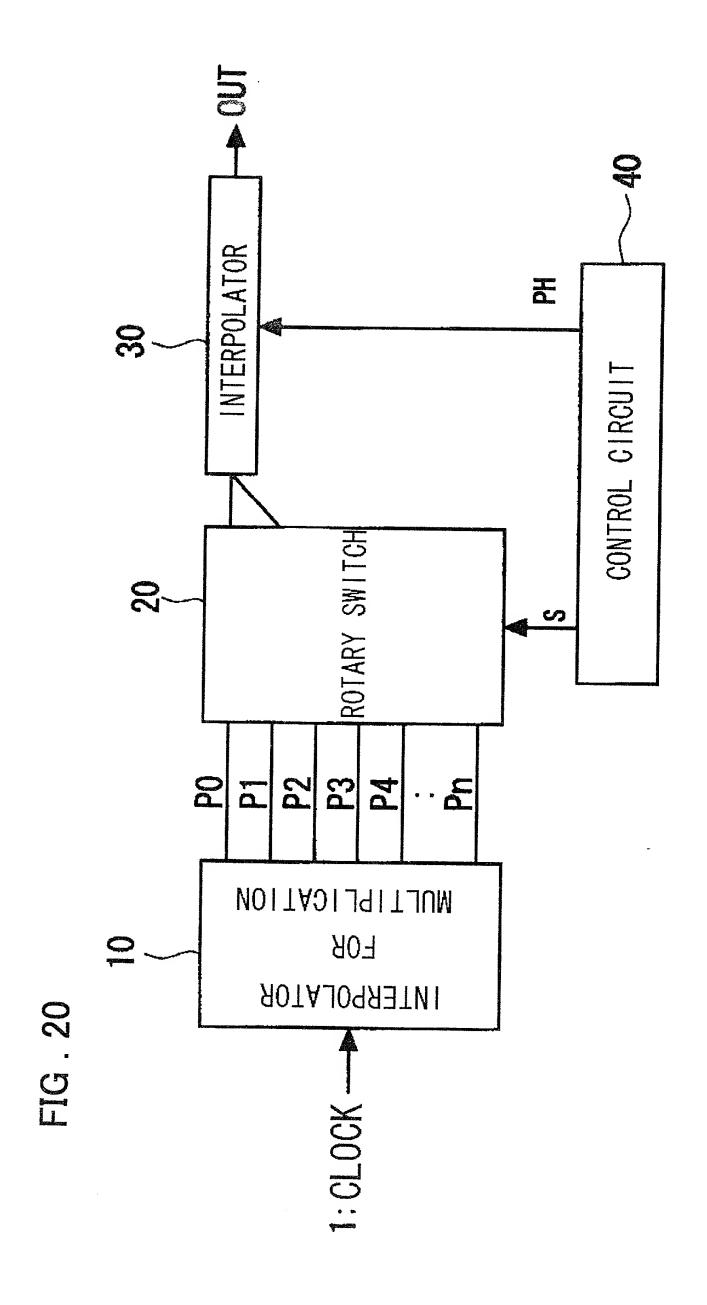
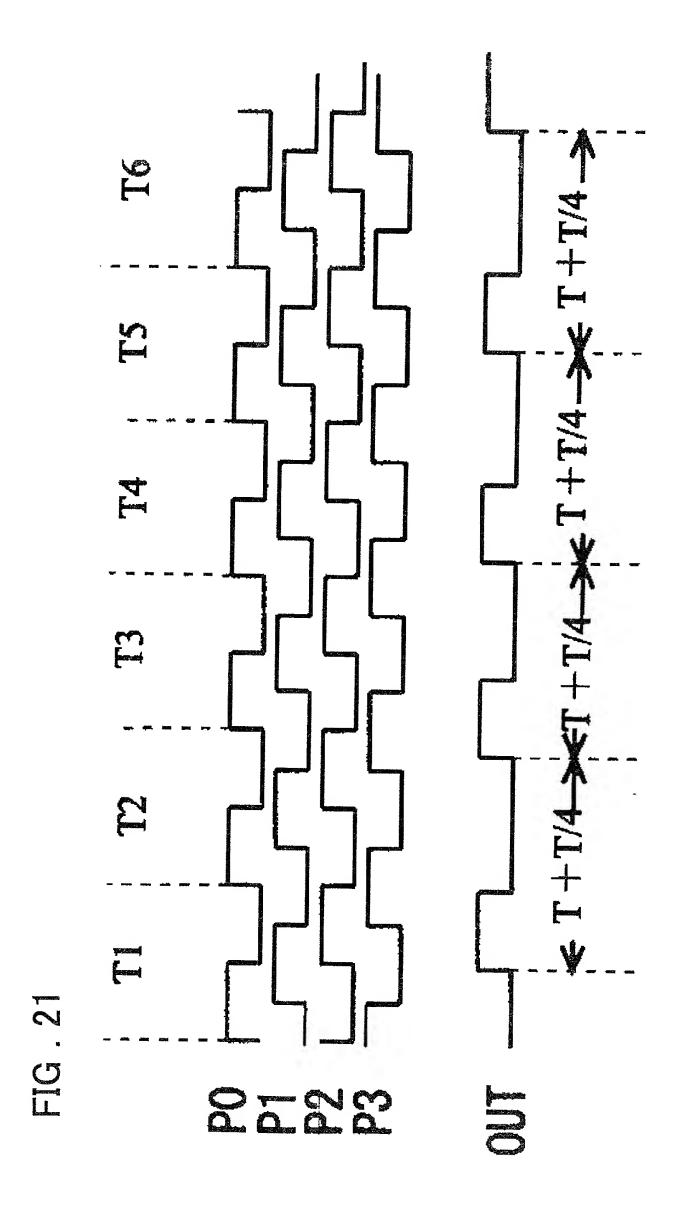


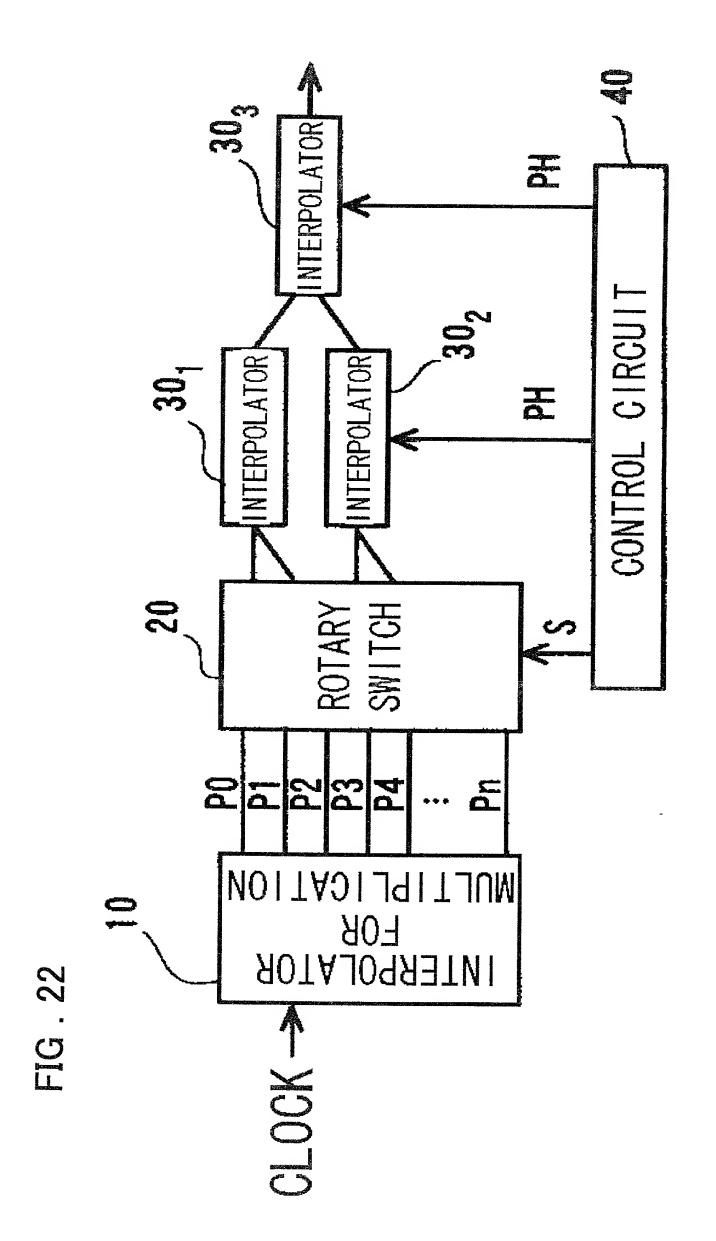
FIG . 18

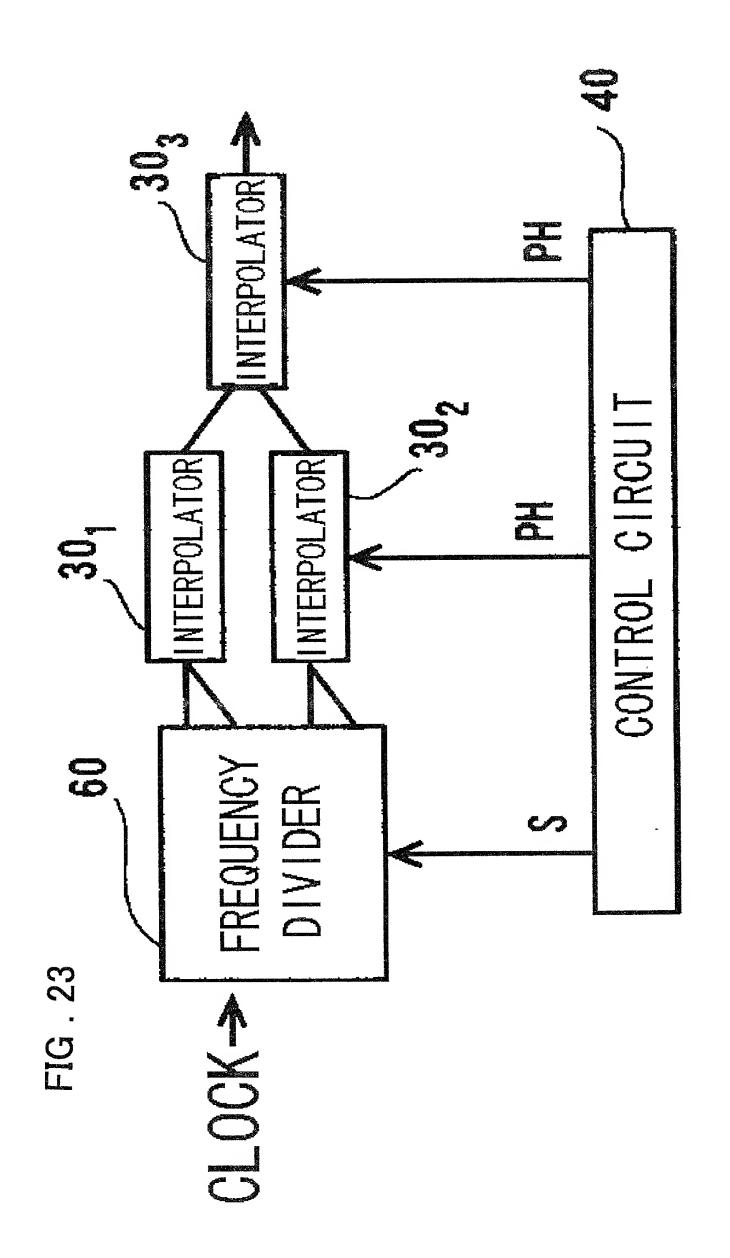












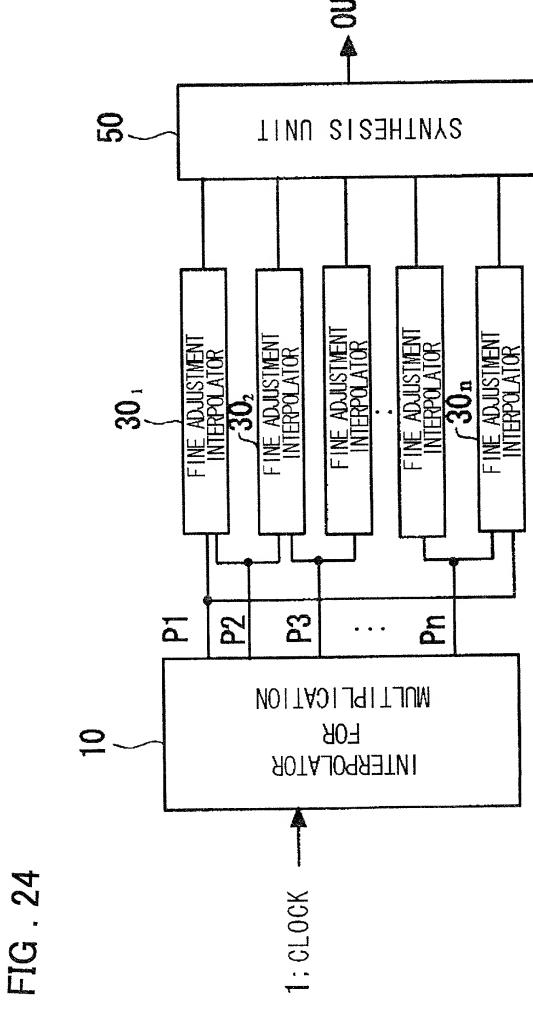


FIG . 25

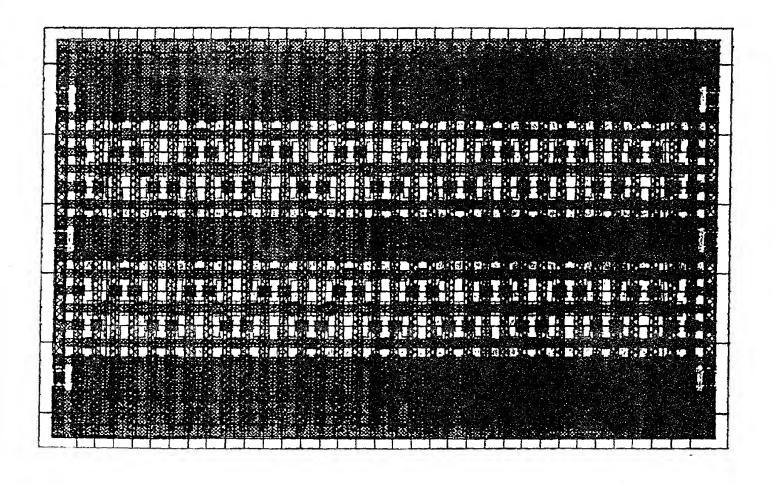


FIG . 26

